



2026 International Conference on Analog VLSI Circuits (AVIC 2026)

Fukuoka, Japan, Oct. 22–23, 2026

Final Program

Organised & Sponsored by



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Conference Time Table

October 22, 2026 (Thursday)

Japan Standard Time (UTC+9)

Start	End	
10:00	11:30	Sightseeing in Fukuoka City
13:00	17:00	Registration (Linkroom2, 4F floor, Daimyo Conference)
13:30	13:40	Opening Ceremony
		Invited Talk
13:40	14:20	Prof. Cosy Muto, Nagasaki University, Japan
		Chair: Prof. Fujihiko Matsumoto
14:20	14:30	Break Time
14:30	15:45	Regular Session 1: RF Circuits
		Chair: Prof. Kawori Sekine
15:45	16:00	Break Time
16:00	17:15	Regular Session 2: Application Circuits for RF 1
		Chair: Prof. Akira Yasuda
17:30	19:30	Banquet (Venue: Linkroom3, 4F floor, Daimyo Conference)

October 23, 2026 (Friday)

Start	End	
9:00	10:15	Regular Session 3: Application Circuits for RF 2 & Analog Circuits 1
		Chair: Prof. Ryoichi Miyauchi
10:15	10:30	Break Time
10:30	11:45	Regular Session 4: Analog Circuits 2 & Nonlinear Analog Circuits
		Chair: Prof. Yasuhiro Takahashi
11:40	12:00	Closing Ceremony
13:00	15:00	Farewell Meeting
		(Traditional Japanese Yakata-bune Boat Cruise in Nakasu)

Invited Talk

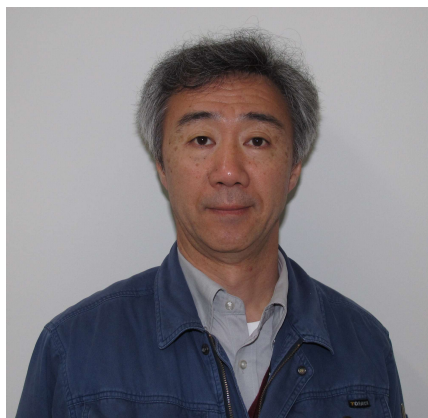
Thursday October 22 13:40—14:20

Chairman: Fujihiko Matsumoto (National Defense Academy)

Speaker Prof. Cosy Muto, Nagasaki University, Japan

Title A Rational Approximation of $\sqrt{5}$ derived from 5th-Order Butterworth *RC* Polyphase Filter

Abstract Engineering draws heavily on the rich fruits of mathematics to model, analyse, and solve real-world problems. However, have we in engineering ever returned the favour to mathematics? In this invited talk, we present a design of a 5th-order Butterworth *RC* polyphase filter with rounded integer-valued resistors, which produces a rational approximation of $\sqrt{5}$ as 161/72. Remarkably, this value perfectly matches classical mathematical methods, including continued fraction expansion, Newton-Raphson iteration, and the ratio of Lucas to Fibonacci numbers. Whether this convergence reflects underlying necessity or coincidence, it reveals an unexpected bridge between analog circuit synthesis and classical number theory. Ultimately, this discovery leads to a clear answer to our opening question: yes, as engineers, we have just returned the favour to mathematics.



Biography Dr. Muto graduated from Takuma National College of Technology, Japan, in 1983. He received B.E., M.E., and Ph.D. degrees in electronics from Nagaoka University of Technology, Japan, in 1985, 1987, and 1994, respectively. He served in the Ground Self-Defense Force as a commissioned technology officer from 1987 to 1998, where, following an initial assignment as a platoon leader, he was engaged in R&D in the field of communications-electronics. He was with Takuma National College of Technology from 1998 to 2001, The Kitakyushu Foundation for the Advancement of Industry, Science and Technology from 2002 to 2004, and Kyushu Institute of Technology from 2004 to 2009. He joined the Faculty of Education, Nagasaki University, Japan, in 2009, where he is currently a Professor. His research includes analogue signal processing and circuits, especially complex analogue filters, and technology education including AI literacy. He is a Senior Member of both IEEJ and IEICE, and a member of IEEE and the Japan Society of Technology Education.

Regular Session

Thursday October 22 14:30–15:45

Session 1: RF Circuits

Chairman: Kawori Sekine (Meiji University)

- A1** A design of high-performance inverter and RGC based transimpedance amplifier
Kento Samura (Gifu University, Japan); Yasuhiro Takahashi (Toyo University, Japan); Daisuke Ito, Makoto Nakamura (Gifu University, Japan)*
- A2** A CMOS folded gilbert cell mixer using derivative superposition method for 2.4 GHz
Kyohei Sota, Ryoichi Miyauchi, Akira Hyogo (Tokyo University of Science, Japan)*
- A3** An Always-on centimeter-resolution IR-UWB radar in 28-nm FD-SOI
Pierre Ferrer, Yann Deval, Hervé Lapuyade, François Rivet (Université de Bordeaux, France)*
- A4** Methodology for fast co-simulation of radio frequency integrated circuits using carrier aggregated signals
Rémi Quéheille, Nathalie Deltimple, François Rivet (Université de Bordeaux, France)*
- A5** A compact feedback-assisted active balun with frequency-selective Complex impedance synthesis in 22 nm FD-SOI
Tomasz Borejko, Witold A. Pleskacz (Warsaw University of Technology, Poland)*

Thursday October 22 16:00–17:15

Session 2: Application Circuits for RF 1

Chairman: Akira Yasuda (Hosei University)

- B1** Single-chip integration of a TIA and a 2-Input multiply-accumulate circuit for an optoelectronic reservoir computing system
Masaki Mizushina, Kawori Sekine, Kazuyuki Wada (Meiji University, Japan); Satoshi Sunada (Kanazawa University, Japan); Shinsuke Hara, Satoru Tanoi, Akifumi Kasamatsu (National Institute of Information and Communications Technology, Japan)*
- B2** Design and evaluation of a dedicated reinforcement learning circuit for 4-channel selection systems
Koshiro Kurisu, Heizo Matsuzaki, Kawori Sekine, Kazuyuki Wada (Meiji University, Japan); Mikio Hasegawa (Tokyo University of Science, Japan); Shinsuke Hara, Satoru Tanoi, Akifumi Kasamatsu (National Institute of Information and Communications Technology, Japan)*
- B3** Evaluation of a learning system incorporating an analog MSE calculation circuit for an optoelectronic reservoir system
Keisuke Kusano, Kawori Sekine, Kazuyuki Wada (Meiji University, Japan); Satoshi Sunada (Kanazawa University, Japan); Shinsuke Hara, Satoru Tanoi, Akifumi Kasamatsu (National Institute of Information and Communications Technology, Japan)*
- B4** Self-driven reverse current Suppression with soft-switching for cross-coupled differential-drive CMOS rectifiers
Takaki Akao, Ryoichi Miyauchi, Akira Hyogo (Tokyo University of Science, Japan)*
- B5** Clock feedthrough reduction technique for synchronized switch harvesting on capacitors
Yusuke Kakinuma, Ryoichi Miyauchi, Akira Hyogo (Tokyo University of Science, Japan)*

Friday October 23 9:00–10:15

Session 3: Application Circuits for RF 2 & Analog Circuits 1

Chairman: Ryoichi Miyauchi (Tokyo University of Science)

- C1** Design of adiabatic logic circuits driven exclusively by an AC power supply
*Shunsuke Goto** (Gifu University, Japan); *Yasuhiro Takahashi* (Toyo University, Japan); *Daisuke Ito*, *Makoto Nakamura* (Gifu University, Japan)
- C2** A new time-constant control circuit for optical burst receivers operating at 25 Gb/s
*Yusuke Kuwahara** (Gifu University, Japan); *Yasuhiro Takahashi* (Toyo University, Japan); *Daisuke Ito*, *Makoto Nakamura* (Gifu University, Japan)
- C3** Investigation of a permittivity measurement method using a frequency-tunable resonator
*Kuniaki Kure**, *Shunya Watanabe*, *Hinata Ito* (Hosei University, Japan); *Yasuhiro Sugimoto* (Chuo University, Japan); *Kiichi Yamashita*, *Akira Yasuda* (Hosei University, Japan)
- C4** A design of a low-frequency 5th-order low-pass notch filter with capacitance multipliers
Fujihiko Matsumoto, *Daichi Shigihara*, *Kanata Yoshida** (National Defense Academy, Japan)
- C5** Verification of FIA time-sharing for low-power EF-NS SAR ADCs in IoT Applications
*Yuya Shimmyo**, *Ryoichi Miyauchi*, *Tetsuji Matsuura*, *Akira Hyogo* (Tokyo University of Science, Japan)

Friday October 23 10:30–11:45

Session 4: Analog Circuits 2 & Nonlinear Analog Circuits

Chairman: Yasuhiro Takahashi (Toyo University)

- D1** Leveraging open-source EDA for low-volume, high-mix LSI development
*Seijiro Moriyama** (Anagix Corporation, Japan); *Chikau Takahashi* (Takamori Co., Ltd, Japan); *Kazuhiro Shouno* (University of Tsukuba, Japan); *Hiroshi Tanimoto* (Kitami Institute of Technology, Japan)
- D2** FPGA implementation of a fully event-driven SNN and performance comparison with an ANN
*Yuga Makitaa**, *Rikuto Nishiyama*, *Hiroyuki Kamata* (Meiji University, Japan)
- D3** Accelerating feature detection for lunar navigation using the low-rank structure of PCA templates
*Taisei Hayashi**, *Hiroki Shoji*, *Hiroyuki Kamata* (Meiji University, Japan)
- D4** Measurement and experimental validation of a 16-armed bandit analog integrated circuit using pseudo slot machines
*Heizo Matsuzaki**, *Kohei Mori*, *Kazuyuki Wada*, *Kawori Sekine* (Meiji University, Japan); *Shinsuke Hara*, *Satoru Tanoi*, *Akifumi Kasamatsu* (National Institute of Information and Communications Technology, Japan)
- D5** Proposal of an auto-zero amplifier with compensation of electrode offset voltage for ECG measurement
*Keisuke Kinoshita**, *Minori Watanabe*, *Hiroshi Endo*, *Ryoichi Miyauchi*, *Akira Hyogo* (Tokyo University of Science, Japan)

Note: * is a presenter.

