# 2022 International Conference on Analog VLSI Circuits (AVIC 2022)

Hiroshima, Japan, Oct. 31st – Nov. 2nd, 2022

# Program

**Organised by**

Institute of Electrical Engineers of Japan

Hiroshima Institute of Technology

Hiroshima Institute of Technologoy

**Sponsored by**

Micron Memory Japan, K.K.

IEEE CASS Japan Joint Chapter

IEEE SSCS Japan Chapter

# Message from General Co-Chair

Since the International Conference on Analog VLSI Circuits (AVIC), formerly, IEEJ International Analog VLSI Workshop was first held at Ohio State University in 1997, AVIC has been held all over the world including Taiwan, Thailand, Ireland, France and Canada. Thanks to everyone's support for AVIC has gained 20+ years of history.

As the COVID-19 epidemic is gradually converging worldwide, AVIC will be held in Japan for the first time this year for the purpose of IEEJ AVIC staff's infection prevention and management.

In AVIC we will discuss a wide range of analog themes based on theory and experience, including not only electronic circuits targeting integrated circuits, but also applications including discrete circuits, evaluation, manufacturing, data analysis, EDA and AI.

In order to overcome the current situation in which the supply of semiconductors cannot keep up with the demand, it is now important to design and develop more efficient semiconductors that take into account not only manufacturing but also design. Against this background, we sincerely hope that semiconductor designers and researchers from all over the world will gather in Japan to share various ideas and contribute to the further development of the semiconductor industry.

Hiroshima, where AVIC 2022 will be held, has many tourist attractions such as Itsukushima Shrines and the Atomic Bomb Dome of UNESCO World Cultural Heritage. Hiroshima also has a rich seafood culture from the Seto Inland Sea.

We hope that, through the AVIC 2022, everyone who attends this conference will have many great cultural experiences and feel the best hospitality in Hiroshima.

Mr. Satoru Shingai
Canon Inc., Japan

Prof. Dr. Toshihiko Hamasaki
Hiroshima Institute of Technology, Japan

# Message from Technical Program Committee Chair

On behalf of the technical committee of the 2022 IEEJ International Conference on Analog VLSI Circuits (AVIC 2022), we welcome you to Hiroshima Institute Technology in the Hiroshima-International City of Peace and Culture. This conference is organized by the Research Committee on Electronic Circuits of the Institute of Electrical Engineers of Japan (IEEJ).

Our technical program this year consists of five analog-related sessions, which are "ADC," "Analog circuits I and II," "Emerging Circuit and Systems," and "RF Communication and Oscillators." The total number of papers is 24, including four invited papers and three keynote speeches.

The present and future of high-speed wireless communication in the millimeter-wave and THz wavebands using CMOS technology will be presented in the keynote speech. On the first day, Prof. Minoru Fujishima will present "300-GHz band transceiver using silicon CMOS integrated circuits". "Millimeter-Wave/THz CMOS Phased-Array Transceiver for 6G" will be presented by Prof. Kenichi Okada on the second day. On the last day, Prof. Stefan Marinca will present "Process Independent Voltage Reference".

The four invited papers related to circuit technology, "A System Perspective to Analog Front-End for Industrial Instrumentation" by Mr. Dai Kato, "Automatic Design/Synthesis of Analog Integrated Circuit using Machine Learning" by Prof. Nobukazu Takai, "Ergodic Sequential Logic Biomimetic Circuits for Hardware-Efficient Medical Engineering Applications" by Prof. Hiroyuki Torikai, "Tiny CMOS towards Big Future" by Prof. Kiichi Niitsu, will be presented.

The AVIC 2022 Technical Program Committee has prepared the technical program. We would like to offer special thanks to the reviewers, the Technical Program members, the keynote speakers, and the invited speakers for developing an outstanding technical program. We look forward to seeing you all in Hiroshima, and let's create a new era after COVID-19 with our technology.

Prof. Dr. Akira Yasuda
Hosei University, Japan

# Organizing Committee

| | |
|---|---|
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# Conference Time Table

**Time: Japan Time Zone (UTC+9)**

| **Monday**<br>**October 31st** | **Tuesday**<br>**November 1st** | **Wednesday**<br>**November 2nd** |
|---|---|---|
| 9:30–10:00<br>**Opening Ceremony** | | |
| 10:00–10:40<br>**Keynote 1**<br>Prof. Minoru Fujishima | 9:30–10:10<br>**Keynote 2**<br>Prof. Kenichi Okada | 9:30–10:10<br>**Keynote 3**<br>Prof. Stefan Marinca |
| 11:10–12:30<br>**Session A.1** | 10:40–12:00<br>**Session B.1** | 10:20–11:20<br>**Poster Session** |
| 12:30–13:50<br>**Lunch** | 12:00–13:40<br>**Lunch** | 12:45–17:00<br>**Technical Visit Tour I&II*** |
| 13:50–14:30<br>**Invited Talk 1** | 13:40–14:20<br>**Invited Talk 4** | 17:00–<br>**Best Paper Award Ceremony in Tour I** |
| 14:40–15:20<br>**Invited Talk 2** | 14:40–15:40<br>**Session B.2** | |
| 15:30–16:10<br>**Invited Talk 3** | 16:00–17:00<br>**Session B.3** | |
| 16:40–17:40<br>**Session A.2** | | |

* Tour I is sponsored by Micron Memory Japan KK. Tour II is subsidized by Hiroshima Convention & Visitors Bureau.

# Keynote

## Monday October 31st 10:00–10:40

### Chairman: Prof. Toshihiko Hamasaki (Hiroshima Institute of Technology)

**Speaker** **Prof. Minoru Fujishima, Hiroshima University, Japan**

**Title** **300-GHz Band Transceiver Using Silicon CMOS Integrated Circuits –Behind-the-Scenes of Circuit Design that Exceeds $f_{\max}$–**

**Abstract** In the 300-GHz band, data rates in excess of 100 Gb/s are expected since the continuous frequency band of 44 GHz can be used for wireless communications. As a result, white papers on 6th generation (6G) or Beyond 5G often refer to the 300-GHz band. 300-GHz is part of the terahertz spectrum between light and radio waves. As a result, 300-GHz band transceivers based on optical mixing were developed first. This was followed by 300-GHz band transceivers based on electronics devices using compound semiconductors. Furthermore, it is desirable to realize it in CMOS integrated circuits, which are suitable for mass production. The unity gain frequency (fmax) of silicon NMOSFETs used in CMOS integrated circuits has been improved by miniaturization, but it peaked in the 65-nm to 28nm generation and remains at around 300 GHz. Under these conditions, we have been working on the realization of a 300-GHz transceiver using full-CMOS circuits. In this presentation, an overview of 300-GHz band communications, circuit technology for 300-GHz band transceivers will be introduced, and the future evolution of sub-THz transceivers including 300-GHz band transceivers will be discussed.

**Biography** Prof. Minoru Fujishima received his Ph.D. from the University of Tokyo in 1993, and after working as an assistant and an associate professor at the University of Tokyo, he has been a full professor at Hiroshima University since 2009. He was a visiting professor at the Katholieke Universiteit Leuven, Belgium, from 1998 to 2000. He was formerly engaged in research on design and modeling of CMOS and BiCMOS circuits, nonlinear circuits, single-electron circuits, and quantum computing circuits, and is currently interested in research on ultrahigh-speed wireless communications using terahertz wave. He served as a distinguished lecturer of the IEEE Solid State Circuits Society, Chair of the IEEE Japan Council Chapter Operations Committee, and is currently President of the Electronics Society of the Institute of Electronics, Information and Communication Engineers. He is a fellow of the Institute of Electronics, Information and Communication Engineers, a senior member of the IEEE, and a member of the Japan Society of Applied Physics.

# Tuesday November 1st 9:30–10:10

## Chairman: Dr. Ryuichi Fujimoto (KIOXIA Corporation)

**Speaker Prof. Kenichi Okada, Tokyo Institute of Technology, Japan**

**Title Millimeter-Wave/THz CMOS Phased-Array Transceiver for 6G**

**Abstract** The microwave communication based on the omnidirectional radiation has been studied for long time, and now we have started using the millimeter-wave directional wireless communication based on the beamforming technique. In this presentation, millimeter-wave and terahertz phased-array transceivers by CMOS technology will be introduced, which are designed for 5G and 6G communication. The talk concludes with a discussion on future directions of wireless communication.

**Biography** Prof. Kenichi Okada received the B.E., M.E., and Ph.D. degrees from Kyoto University, Kyoto, Japan, in 1998, 2000, and 2003, respectively. He joined Tokyo Institute of Technology in 2003, and he is now a Professor. He has authored and co-authored more than 500 journal and conference papers. His current research interests include millimeter-wave/terahertz wireless transceiver, digital PLL, and ultra-low-power RF circuits. He has worked as a TPC member of ISSCC, VLSI Circuits, and ESSCIRC, RFIC Symposium, A-SSCC, Guest Editors and Associate Editor of JSSC and T-MTT, a Distinguished Lecturer of SSCS.

# Wednesday November 2nd 9:30–10:10

## Chairman: Mr. Satoru Shingai (Canon Inc.)

**Speaker Prof. Stefan Marinca, Technical University of Cluj-Napoca, Romania**

**Title Process Independent Voltage Reference**

**Abstract** Voltage references are essential analog blocks in many Integrate Circuits (IC) like analog to digital (ADC) and digital to analog (DAC) converters, voltage regulators, multipliers, and in a large variety of measurement systems. The most common used silicon-based voltage references are based on BANDGAP concept. The accuracy of any converter is limited by the accuracy of the voltage reference. Bandgap type voltage references are based on the idea that the base-emitting voltage of a bipolar transistor extrapolated to absolute zero, denoted $V_{G0}$, is a fixed voltage. As is actually known, this voltage varies in the order of percentages from device to device even on the same wafer. Other parameters of the bipolar transistor, primarily saturation current temperature exponent, denoted $X_{TI}$, also have variations from device to device. In this paper is presented a new concept, NON-BANDGAP voltage reference, according to which the target of the reference is a voltage that can be measured with a prediction limited only by the adjustment resolution.

**Biography** Prof. Stefan Marinca is currently an expert consulting professor for Technical University of Cluj-Napoca, Romania, vice-president of the Analog Design Services, Ireland, and Chair of the Romanian IEEE Solid State Circuits Society. From 1987 to 2000 he held different academic positions from assistant to associate professor and head of the electronic department at Nord University of Baia Mare Romania. He was also president of the Maramures County Inventor's Society, Romania and founder president of the EU PHARE Program for Developing Small and Medium-Sized Enterprises, CDIMM Maramures. He was the sole founder of the first Romanian private company after the fall of communism in 1990, which invented a novel electrical power measurement device which was launched onto the market in 1990. In 2000 he joined Analog Devices, Inc, a world leading supplier of mixed signal semiconductor devices, as a senior analog designer specializing in voltage references and analog-related sub-circuits at their Limerick, Ireland division. From 2008–2013 he worked for the Santa Clara, California, Division as a Staff Design Engineer. While there he established himself as one of the leading worldwide designers of voltage references, culminating in the award of Innovation of the Year in 2014, and had the opportunity to work with several of the world visionaries of the semiconductor industry such as Paul Brokaw and the late Barrie Gilbert. In 2018, he joined Infineon's Romanian branch at Cluj-Napoca, where he served as a leading designer of analog power systems including LDOs, amplifiers, and temperature sensors. In 2020 he co-founded Analog Design Services, Ltd. Throughout his career, Stefan's innovations in the analog and mixed signal domain have been recognized by numerous patents. He is primary inventor on 36 U.S. granted patents, as well as 17 Romanian patents.

# Invited Talk

## Monday October 31st 13:50–14:30

### Chairman: Prof. Kazuhiro Shouno (University of Tsukuba)

**Speaker** **Mr. Dai Kato, Yokogawa Electric Corporation, Japan**

**Title** **A System Perspective to Analog Front-End for Industrial Instrumentation**

**Abstract** We have developed a compact isolated input analog front-end (AFE) for industrial instrumentation. AFEs convert thermocouples, RTDs, and voltages into digital signals and provide measurements to the instrument system. Large-scale and complex mixed-signal circuit technology is essential to obtain the required stable measurement accuracy. Because the technology is multi-layered from physical layer to logical layer, it is difficult to design with a flat concept. We will introduce an architecture design case using a system perspective to optimize the close relationship between technology layers.

**Biography** Mr. Dai Kato is a Senior Analog Expert / Manager at Yokogawa Electric Corporation, Tokyo Japan. He received his B.E. in Electrical and Electronics from Sophia University in 1988 and he joined Yokogawa Electric Corporation. He has been engaged in research and development of analog and mixed-signal VLSI for industrial and measurement systems, including industrial System on Chip (SoC), reconfigurable systems, digital signal processing, data converters, power converters, high precision timing generators, and sensor interface circuits. He is a member of IEEJ Research Committee of Electronics Circuits, and the Japan Society of Applied Science.

## Monday October 31st 14:40–15:20

### Chairman: Prof. Hao San (Tokyo City University)

**Speaker** **Prof. Nobukazu Takai, Kyoto Institute of Technology, Japan**

**Title** **State-of-the-Art of Automatic Synthesis of Analog Integrated Circuits**

**Abstract** The automatic design of integrated circuits is attracting attention as a means of reducing costs through efficient design and is being developed to incorporate state-of-the-art algorithms

and technologies. Applying machine learning to the automatic design/synthesis of analog integrated circuits is one of the attractive methods to solve the problem. This paper introduces methods for using machine learning in the analog integrated circuit design flow. We will discuss circuit topology selection and circuit synthesis to meet the specifications. Once automatic design/synthesis of analog integrated circuits is achieved, integrated circuit design will move to the next stage, and integrated circuits never seen before will emerge.

**Biography** Prof. Nobukazu Takai received the B.E. and M.E. degrees from Tokyo University of Science, Tokyo , Japan, in 1993, and 1995, respectively and Ph.D. degree from Tokyo Institute of Technology, Tokyo, Japan, in 1999. After working as an assistant professor at Tokyo Polytechnic University and associate professor at Gunma University, he is now a Professor at Kyoto Institue of Technology. He engaged in the research of DC-DC Converter, analog filters, and analog integrated circuit design and now his main interest lies in the field of automatic design/synthesis design of analog integrated circuit using machine learning. Prof. Takai is a member of the Institute of Electrical Engineers of Japan (IEEJ), the Institute of Electronics, Information and Communication Engineers (IEICE), and the Institute of Electrical and Electronics Engineers (IEEE).

## Monday October 31st 15:30–16:10

### Chairman: Prof. Kawori Sekine (Meiji University)

**Speaker Prof. Hiroyuki Torikai, Hosei University, Japan**

**Title Ergodic Sequential Logic Biomimetic Circuits for Hardware-Efficient Medical Engineering Applications**

**Abstract** In this presentation, our recent research projects on ergodic sequential logic (SL) biomimetic circuits are reviewed. First, mathematical backgrounds and practical advantages of the ergodic SL biomimetic circuits are explained. Second, recent examples and potential applications of the ergodic SL biomimetic circuits (e.g., cochlear implant circuit, brain implant circuit, assist device for rehabilitation of walking, hardware-based genome simulator for personalized medicine and personalized drag discovery) are reviewed. Finally, important problems for developing future high-performance and hardware-efficient implantable medical engineering devices are discussed.

**Biography** Prof. Hiroyuki Torikai received the B.E., M.E., and Ph.D. degrees in electrical engineering from Hosei University, Tokyo, Japan, in 1995, 1997, and 1999, respectively. He is currently a Professor with the Faculty of Science and Engineering, Hosei University. His current research interests include bio-engineering, nonlinear dynamics, and neural networks.

## Tuesday November 1st 13:40–14:20

### Chairman: Prof. Kazuyuki Wada (Meiji University)

**Speaker Prof. Kiichi Niitsu, Kyoto University, Japan**

**Title Tiny CMOS towards Big Future –Sub-mm$^2$, Sub-nW CMOS Analog VLSI for Stand-Alone Energy-Autonomous Continuous Glucose Monitoring Contact Lenses–**

**Abstract** As CMOS technology scaling progresses, the required footprint and power for one function has been reduced. This trend enables developing tiny area/power CMOS VLSIs for various applications. This talk presents the latest result on the work on Glucose-fuel-cell-operated Glucose sensing system which can be applied to stand-alone energy-autonomous continuous Glucose monitoring system (CGMS) contact lenses. The work shows world's lowest power consumption sub-mm$^2$ supply-modulated CMOS On-Off Keying (OOK) transmitter for enabling self-powered continuous glucose monitoring contact lens. By introducing self-oscillating voltage doubler and charge pump, compact, low-voltage, low-power supply-modulated OOK transmitter become available. By prototyping 385$\mu$m $\times$ 385$\mu$m testchip in 65-nm CMOS, 0.27 nW under 0.165 V performance and self-powered operation using 2mm $\times$ 2mm solid-state glucose fuel cell were successfully demonstrated. In addition, the talk demonstrates solar-cell-powered bio-fuel-cell-associated CGMS smart contact lenses with LED driving capability.

# Regular Session

## Monday October 31st 11:10–12:30

**Session A1: Analog to Digital converters (ADC)**

**Chairman: Prof. Nobuhiko Nakano (Keio University)**

**A1.1** Reducing one operational amplifer in an 8-bit third-order noise-shaping successive approximation register analog-to-digital converter with error-feedback structure
*Whichan Bae*, Ryo Kishida, Tatsuji Matsuura, Akira Hyogo (Tokyo University of Science)*

**A1.2** Low power multistate ADC for ultrasonic detection and audio band signal processing by OTA-sharing
*Uta Kobayashi*, Sota Mizuno, Akira Yasuda (Hosei University)*

**A1.3** Proposal for a feedback-type digital direct-drive speaker system using an error amplifier circuit
*Konosuke Sakaki*, Satoshi Saikatsu, Yoshihiko Fukawa, Akira Yasuda (Hosei University)*

**A1.4** 0.18 $\mu$m analog/PWM/digital converter with pulsed temperature compensation using sub-threshold region
*Tomichika Harada* (Yamagata University)*

## Monday October 31st 16:40–17:40

**Session A2: Analog Circuit I**

**Chairman: Mr. Go Urakawa (KIOXIA Corporation)**

**A2.1** Enabling signal input and output by voltage and reducing circuit area for exponentiation conversion IC
*Fumiya Matsui*, Naoya Nishiyama, Yuji Sano (Toyo University)*

**A2.2** Process independent voltage reference
*Stefan Marinca* (Technical University of Cluj-Napoca)*

**A2.3** Simulation analysis of newly designed overshoot current detection circuit for IGBTs
*Tomoya Omoto*, Satoshi Sugahara (Fukuyama University)*

## Tuesday November 1st 10:40–12:00

**Session B1: RF communications and Oscillators**

**Chairman: Prof. François Rivet (Université de Bordeaux)**

**B1.1** A 40 GHz varactor-less class-C VCO with 17.1% tuning range and long-term reliability in 28nm FD-SOI for satellite communications
*Ayoub Ait Ihda (IMS Laboratory, Univ. Bordeaux, CNES.); Yann Deval *; Hervé Lapuyade, François Rivet (Univ. Bordeaux); Matthieu Gastaldi (CNES); Stephane Rochette (Thales Alenia Space)*

**B1.2** A 27.2-27.8 GHz fine frequency tuning DCO using 13-bit switched resistor
*Naoto Tamura*, Kiyotaka Komoku, Nobuyuki Itoh (Okayama Prefectural University)*

**B1.3** Commercial power supply synchronous low-frequency oscillator circuit using on-chip solar cell
*Kenta Yamamura, Yuta Watanabe, Siun Yamakiri, Nobuhiko Nakano (Keio Univsersity)*

**B1.4** Burst-mode driver circuit with on-chip bias tee for in-Vehicle optical networks
*Daisuke Ito*, Yasuhuiro Takahashi, Makoto Nakamura (Gifu University); Toshiyuki Inoue, Akira Tsuchiya, Keiji Kishine (The University of Shiga Prefecture)*

## Tuesday November 1st 14:40–15:40

**Session B2: Emerging Circuits and Systems**

**Chairman: Prof. Nobuyuki Itoh (Okayama Prefectural University)**

**B2.1** Minimal Fab PDK enpowered by Open PDK technology
*Seijiro Moriyama* (Anagix Corporation); Michitaka Yoshino (Hosei University); Kazuhiro Shouno (University of Tsukuba); Hiroshi Tanimoto (Kitami Institute of Technology)*

**B2.2** Variable-filter stability guarantee employing unity-bounded functions
*Tian-Bo Deng* (Toho University)*

**B2.3** Tolerance in reinforcement learning systems for analogue history storage circuits implemented in 180 nm CMOS process
*Haruto Unno*, Kawori Sekine, Kazuyuki Wada (Meiji University); Shinsuke Hara, Akifumi Kasamatsu, Satoru Tanoi (National Institute of Information and Communications Technology); Makoto Naruse (The University of Tokyo)*

## Tuesday November 1st 16:00–17:00

**Session B3: Analog Circuits II**

**Chairman: Prof. Nicodimus Retdian (Shibaura Institute of Technology)**

**B3.1** Low-voltage CMOS continuous-time integrator with capacitance multiplier
*Hiroki Sato*, Shigetaka Takagi (Tokyo Institute of Technology)*

**B3.2** Tolerance analysis of comparator noise for ultrafast photonic reinforcement learning
*Hiroki Iwahara*, Kawori Sekine, Kazuyuki Wada (Meiji University); Makoto Naruse (The University of Tokyo); Shinsuke Hara, Akifumi Kasamatsu, Satoru Tanoi (National Institute of Information and Communications Technology)*

**B3.3** Increasing the speed of environmental adaptation using nonlinear characteristic on analog history storage circuit
*Haruto Unno*, Kawori Sekine, Kazuyuki Wada (Meiji University); Shinsuke Hara, Akifumi Kasamatsu, Satoru Tanoi (National Institute of Information and Communications Technology); Makoto Naruse (The University of Tokyo)*

**Note:** * is a presenter.

# Poster Session

## Tuesday November 2nd 10:20–11:20

9 papers has been nominated for the Best Paper Award. The session is held for winner selection process. The winners will be recognized publicly at the Best Paper Award Ceremony.

**A1.1** Reducing one operational amplifer in an 8-bit third-order noise-shaping successive approximation register analog-to-digital converter with error-feedback structure
*Whichan Bae*, Ryo Kishida, Tatsuji Matsuura, Akira Hyogo (Tokyo University of Science)*

**A1.2** Low power multistate ADC for ultrasonic detection and audio band signal processing by OTA-sharing
*Uta Kobayashi*, Sota Mizuno, Akira Yasuda (Hosei University)*

**A2.1** Enabling signal input and output by voltage and reducing circuit area for exponentiation conversion IC
*Fumiya Matsui*, Naoya Nishiyama, Yuji Sano (Toyo University)*

**A2.2** Process independent voltage reference
*Stefan Marinca* (Technical University of Cluj-Napoca)*

**B1.1** A 40 GHz varactor-less class-C VCO with 17.1% tuning range and long-term reliability in 28nm FD-SOI for satellite communications
*Ayoub Ait Ihda (IMS Laboratory, Univ. Bordeaux, CNES.); Yann Deval *; Hervé Lapuyade, François Rivet (Univ. Bordeaux); Matthieu Gastaldi (CNES); Stephane Rochette (Thales Alenia Space)*

**B1.2** A 27.2-27.8 GHz fine frequency tuning DCO using 13-bit switched resistor
*Naoto Tamura*, Kiyotaka Komoku, Nobuyuki Itoh (Okayama Prefectural University)*

**B1.3** Commercial power supply synchronous low-frequency oscillator circuit using on-chip solar cell
*Kenta Yamamura, Yuta Watanabe, Siun Yamakiri, Nobuhiko Nakano (Keio Univsersity)*

**B2.1** Minimal Fab PDK enpowered by Open PDK technology
*Seijiro Moriyama* (Anagix Corporation); Michitaka Yoshino (Hosei University); Kazuhiro Shouno (University of Tsukuba); Hiroshi Tanimoto (Kitami Institute of Technology)*

**B3.1** Low-voltage CMOS continuous-time integrator with capacitance multiplier
*Hiroki Sato*, Shigetaka Takagi (Tokyo Institute of Technology)*

**Note:** * is a presenter.